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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/042,102	01/07/2002	Michael John Mayfield	AUS920010808US1	6878

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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/042,102	MAYFIELD ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) __ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *1/7/02* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date __.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 10, and 23 are objected to because of the following informalities:

In claim 10, line 3, "Z(1 to 2)", and line 4, "Z(1 to 2)+1" were not well defined. It is suggested to clearly describe "Z(1 to 2)", and "Z(1 to 2)+1" in the claim. Similar problems exist in claim 23.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 2, 3, 5, 6, 8, 9, 14, 15, 17, and 18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

In claims 2, 5, 8, 14, and 17, Data Stream Touch(DST); and in claims 3, 6, 9, 15, and 18, VMS system architecture were not described in the specification.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, lines 7-8, it is not clear what is meant by "the appropriate modified hardware prefetch mechanism" since how

to define an "appropriate" modified hardware prefetch mechanism was not described previously.

In claims 2, 5, 8, 14, and 17, Data Stream Touch(DST); and in claims 3, 6, 9, 15, and 18, VMS system architecture were not described in the specification. Therefore, the real limitations of the claims are unable to be defined.

In claim 4, lines 4-5, it is not clear what is meant by "whether the software prefetch instruction is within a set of predetermined values" since a software prefetch instruction can not be a predetermined value.

In claim 7, h), it is not clear what is meant by "for software prefetch mechanisms not within steps a through g". The software prefetch mechanisms are the destination of mapping from software prefetch instructions. It is suggested to change "for software prefetch mechanisms not within steps a through g" to -if the values in said fields of software prefetch instructions are not within the values specified in steps b through g-.

In claim 13, e), it is not clear what is meant by "if the values of the software prefetch instruction are not the set of predetermined comparison values" since a software prefetch instruction can not be a value.

In claim 16, i), it is not clear what is meant by "whether the software prefetch instructions are not within the values

specified" since a software prefetch instruction can not be a value. Similar problems exist in the other claim 22, h).

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-6, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Snyder (U.S. Patent No. 6,073,215) (hereafter referred to as Snyder'215).

Referring to claim 1, Snyder'215 discloses, as claimed, a method for efficiently utilizing resources in a data processing system employing software and hardware data prefetching instruction mechanisms, the method comprising:

a) mapping a subset (see Col. 6, lines 58-63, BLOCK SIZE 104 is stored in register 312, BLOCK COUNT 106 is stored in register 314, and BLOCK STRIDE 108 is loaded into register 316) of the software prefetch instructions (DST Instruction 100, see Fig. 2, see also Col. 6, lines 57-63, regarding "when used to execute DST instruction 100, BLOCK SIZE 104 is stored in register 312, BLOCK COUNT 106 is stored in register 314, and BLOCK STRIDE 108 is loaded into register 316. State machine/adder 302 receives both the effective address indicated by EA 110 and the contents of DST registers 310") to a modified version of the hardware prefetch mechanism (DST hardware 300, see Fig. 3 and Col. 4, line 17-18); and

b) executing a software prefetch instruction (DST Instruction 100, see Fig. 2) within the subset of included software prefetch instructions by invoking the appropriate modified hardware prefetch mechanism (DST hardware 300, see Fig. 3 and Col. 4, line 17-18). Note as set forth above, see also Col. 6, lines 57-63, regarding "when used to execute DST instruction 100, BLOCK SIZE 104 is stored in register 312, BLOCK COUNT 106 is stored in register 314, and BLOCK STRIDE 108 is loaded into register 316. State machine/adder 302 receives both the effective address indicated by EA 110 and the contents of DST registers 310".

As to claims 2 and 5, Snyder'215 also discloses: the software prefetch instructions are Data Stream Touch (DST) instructions (DST Instruction 100, see Fig. 2).

As to claims 3 and 6, Snyder'215 also discloses: as best understood, the hardware prefetch mechanism (DST hardware 300, see Fig. 3 and Col. 4, line 17-18) is a part of a VMX system architecture (since virtual memory management unit MMU 16 is used, see Fig. 1).

Referring to claim 4, Snyder'215 discloses, as claimed, a method of operating a data processing system in response to a software prefetch instruction, the method comprising:

a) decoding (the decoding step is deemed to be inherent before an instruction is executed) the software prefetch instruction (DST Instruction 100, see Fig. 2);

b) responsive to the decoding, determining whether the software prefetch instruction is within a set of predetermined values for each field within the instruction (note within software prefetch instruction 100, the BLOCK SIZE 104 is stored in register 312, BLOCK COUNT 106 is stored in register 314, and BLOCK STRIDE 108 is loaded into register 316. However, it is deemed to be inherent that before the storings, the space

(equivalent to a predetermined value) of the DST registers 312, 314, and 316 are determined in order to avoid overflow);

c) if the software prefetch instruction is within the set of predetermined values (if not, then an exception such as overflow will occur and the following mapping step will not be executed), mapping (see Col. 6, lines 58-63, BLOCK SIZE 104 is stored in register 312, BLOCK COUNT 106 is stored in register 314, and BLOCK STRIDE 108 is loaded into register 316) the decoded software prefetch instruction to a hardware prefetch mechanism (DST hardware 300, see Fig. 3 and Col. 4, line 17-18); and

d) invoking the hardware prefetch mechanism (DST hardware 300, see Fig. 3 and Col. 4, line 17-18) to perform the software prefetch instruction (DST Instruction 100, see Fig. 2, see also Col. 6, lines 57-63, regarding "when used to execute DST instruction 100, BLOCK SIZE 104 is stored in register 312, BLOCK COUNT 106 is stored in register 314, and BLOCK STRIDE 108 is loaded into register 316. State machine/adder 302 receives both the effective address indicated by EA 110 and the contents of DST registers 310").

Referring to claim 13, Snyder'215 discloses, as claimed, an apparatus for executing data prefetch instructions in a computer system having a memory, the apparatus comprising:

a) a set of software prefetch instruction field parameters comprising Block Count (106, see Fig. 2), Block Size (104, see Fig. 2) and Stride parameters (108, see Fig. 2) stored in the memory (see Col. 5, lines 28-30) of the computer system;

b) a range of predetermined comparison values for Block Count (106, see Fig. 2), Block Size (104, see Fig. 2) and Stride (108, see Fig. 2) fields stored in the memory of the computer system (see Col. 5, lines 48-52, regarding "In one embodiment, BLOCK SIZE 104 is a five-bit field, allowing from 1 to 32 blocks of vector bytes, BLOCK COUNT 106 is an eight-bit field allowing 1 to 256 blocks to be fetched, and BLOCK STRIDE 108 is a signed 16-bit field allowing .+-.32,768 bytes of stride";

c) means for decoding (means for the decoding step is deemed to be inherent since an instruction needs to be decoded before being executed) the software prefetch instruction (DST Instruction 100, see Fig. 2) the software prefetch instruction fields;

d) means for comparing the values in the Block Count, Block Size, and Stride fields of the software prefetch instruction to the set of predetermined comparison values (the predetermined

bit number) for the Block Count, Block Size, and Stride fields (note within the software prefetch instruction 100, the BLOCK SIZE 104 is stored in register 312, BLOCK COUNT 106 is stored in register 314, and BLOCK STRIDE 108 is loaded into register 316 . It is deemed to be inherent to compare the values in the Block Count, Block Size, and Stride fields with the space (equivalent to a predetermined value) of the DST registers 312, 314, and 316 respectively before they are stored therein to avoid overflow);

e) means for mapping (see Col. 6, lines 58-63, within the software prefetch instruction 100, the BLOCK SIZE 104 is stored in (or mapped to) register 312, BLOCK COUNT 106 is stored in (or mapped to) register 314, and BLOCK STRIDE 108 is loaded into (or mapped to) register 316) the decoded software prefetch instruction to a hardware prefetch mechanism if the values of the software prefetch instruction are within the set of predetermined comparison values (if not, then an exception such as overflow will occur and the mapping step will not be executed); and

f) means for invoking the hardware prefetch mechanism to perform the software prefetch instruction (DST Instruction 100, see Fig. 2, see also Col. 6, lines 57-63, regarding "when used to execute DST instruction 100, BLOCK SIZE 104 is stored in register 312, BLOCK COUNT 106 is stored in register 314, and

BLOCK STRIDE 108 is loaded into register 316. State machine/adder 302 receives both the effective address indicated by EA 110 and the contents of DST registers 310").

Allowable Subject Matter

8. Claims 7, 10-12, 16, and 19-25 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

9. The following is a statement of reasons for the indication of allowable subject matter: Snyder'215, the closest reference, and the other prior art do not teach or fairly suggest: in steps c-h of claim 7, using the specific value of Block Count field (such as 1) and Stride field (such as represent the number of 128 bytes) to control the mapping and not mapping between the software prefetch instruction and the hardware prefetch mechanism. Claim 16 steps c-i and claim 22 steps c-h recite the corresponding limitations as set forth in claim 7. The combination of the above limitations and all of the other limitations in the respective independent claim is not obvious.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Stone et al.'260 discloses a method for prefetching structured data, and more particularly a mechanism for observing address references made by a processor, and learning from those references the patterns of accesses made to structured data; Scales III et al.'130 discloses: as illustrated in FIG. 2, DST instruction 100 includes a plurality of fields, including an op code 102 labeled "DST0", a BLOCK SIZE 104, a BLOCK COUNT 106, a BLOCK STRIDE 108, a STRIDE MODIFIER 116, and an effective address field (EA) 110. In a preferred embodiment, BLOCK SIZE 104 is a five-bit field, allowing from 1 to 32 blocks of vector bytes, BLOCK COUNT 106 is an eight-bit field allowing 1 to 256 blocks to be fetched, and BLOCK STRIDE 108 is a signed 16-bit field allowing +-.32,768 bytes of stride; McInerney et al.'134 discloses: a computer processor with a mechanism for improved prefetching of instructions into a local cache includes an instruction pointer multiplexer that generates one of a plurality of instruction pointers in a first pipeline stage, which is used to produce a physical address from an ITLB lookup; and Emberson discloses: an

instruction-level method and system for prefetching data or instructions of variable size to specified cache sets. A prefetch instruction containing binary fields allows the compiler, loader or runtime software to control cache prefetching and reduce thrashing by providing the prefetch hardware with information as to the optimal cache set location and the optimal amount of data to be prefetched.

Contact Information

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

12. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number:** 703-872-9306.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER
August 31, 2004